Objective:
The purpose of this laboratory exercise is to introduce you to data converter circuit design. In this lab, you will implement both analog to digital converter and digital to analog converter.

Equipment Usage
For this lab the following equipment will be used:
- LM324, LM339
- Power supply
- Multi-meter
- Breadboard
- Oscilloscope
- Function Generator
- 10X probe.

Background:
Digital-to-Analog converters (DACs) and Analog-to-Digital converters (ADC) are important building blocks for interfacing real world signal to digital world. An ADC takes an analog signal and converts it into a binary one, while a DAC converts a binary signal into an analog value. Figure 9-1 shows a block diagram of such a system.

Figure 9-1
Analog to Digital Converter (ADC) converts a continuous time signal to discrete time signal. The input-output relationship of an ADC is shown in Figure 9-2 for a 3-bit converter. Notice that when the analog input signal (on the horizontal axis) reaches a certain level, a new digital code will be generated (see vertical axis in Figure 9-2b) which represents the digital output of the ADC as a function of the analog input. The maximum analog signal the ADC can accommodate is called the Full Scale (FS) as is shown in Fig. 2b. As an example, if the analog input is equal to 4/8xFS (Full Scale), the output code for the example of Figure 9-2b will be (100). However, if one increases the magnitude of the input signal above 4.5/8xFS, the new digital output code will be (101).

![Figure 9-2](image)

Prior to conversion of signal, continuous time signal must be sampled and follow the Nyquist-Shannon sampling theorem:

- An analog signal that is sampled at constant intervals can be accurately reconstructed so long as the range of frequencies in the signal is small enough.
- Sampling frequency must be twice the bandwidth of the signal.
- To reconstruct original signal, SINC interpolation is used to fill-in time between samples.

After the continuous time signal is sampled, a quantizer produces a finite number of outputs (e.g., 0–255). The resolution of the quantizer is the number of possible output values. There are many types of ADC i.e. flash, pipelined, successive approximation, etc. In this lab, we will be working with flash converter. A flash converters’ basic operation is based on comparing two input voltages. If input signal voltage is lower than the reference voltage, then the output is low. Otherwise, output is high.

Obviously, for one input and one comparison the usefulness of this technique is quite limited. However, by building a series of comparisons each at a slightly different voltage, one can determine some level of quantization of the input voltage. A simple ADC quantizer is shown on Figure 9-3 and Figure 9-4. Note that Op Amp LM324 acts as a comparator since it does not have any feedback. As a result, if the + terminal is more
positive than the – terminal then the output will be high and if the – terminal is more positive than the – then the output will be all the way low.

On the left side of the comparator sequence is a resistor ladder that generates reference voltages, which are connected to negative terminal of the comparators. If the voltage at the negative terminal of the lowest Op Amp is lower than the input signal, then that Op Amp will have a low output. As the signal rises above that level, the Op Amp will switch to High. As the signal rises, the next Op Amp will switch. As signal increases further, this process continues and Op Amps at higher levels will switch. It should be noted that a linear step ladder is presented here, but any type of step is possible. One such example is a log converter.

After signal comparison is performed, a bubble correction error circuit removes logic error. Bubble error correction is a digital correction mechanism that will prevent a comparator that has tripped high from outputting a high code if it is surrounded by comparators that have not tripped high. Finally, a digital encoder encodes comparators outputs to digital codes. A complete schematic of a 2-bit flash ADC is shown on Figure 9-4.

Figure 9-3: A to D Converter
Design Notes: Resolution of the ADC is limited by the mismatch of the resistor and speed of the ADC is limited by the unity gain frequency of the comparator.

Digital to Analog Converter (DAC) performs the reverse operation of ADC. DAC converts a digital (usually binary) code to an analog signal (current, voltage or electric charge). The input to a DAC is a binary word of n-bits and the output is an analog value, as schematically shown in Figure 9-5.
There are many types of DAC such as current summing, oversampled, R-2R, etc. In this lab, we would use a current summing DAC. Figure 9-6 illustrates a current summing DAC.

This Op Amp is configured as an adder circuit. In addition you do not need to supply a negative supply voltage to any component but rather apply a ground. The reason for this is that with a -12 volt output of the first stage, it will adversely affect the current flow into the adder stage. If you choose to make this a full converter, then a suggested change would be to add a 1N914 diode to the right of the 8kΩ resistors. Then the negative supply voltages must be included.

**Prelab:**
Analysis 1: Design and simulate a 3-bit flash ADC with full scale of 1V. Calculate and simulate quantization levels, quantization noise, SINAD, SNDR, dynamic range and maximum operating frequency. What limits increase of resolution (i.e. number of bits)?
Simulate resolution for 10% mismatch. In addition, calculate and simulate relationship between speed of the converter with that of the unity gain of the opamp/comparator.

**Analysis 2:** Design and simulate a 3-bit current summing DAC with full scale of 1V. Calculate and simulate quantization levels, quantization noise, SINAD, SNDR, dynamic range and maximum operating frequency. What limits increase of resolution (i.e. number of bits)?

**Analysis 3:** Design and simulate an 8-bit R-2R ADC and DAC with full scale of 1V. Calculate and simulate quantization levels, quantization noise, SINAD, SNDR, dynamic range and maximum operating frequency. What limits increase of resolution (i.e. number of bits)?

**Pre-Lab Deliverables:**
1) Submit your completed analysis, schematics and simulation results.
2) Define resolution, aliasing, Nyquist rate, oversampling, monotonicity, offset error, dynamic non-linearity (DNL), integrated non linearity (INL), quantization error, SNDR, SINAD, dynamic range and SFDR.
3) Compare performance of different types of ADCs.
4) Compare performance of different types of DACs.

**Lab Experiments:**

**Experiment 1:** Construct the 3-bit ADC with full scale of 1V and maximum input signal frequency of 6 KHZ. Capture voltage waveforms at the significant circuit nodes to show operation of the circuit.

**Experiment 2:** Construct the 8-bit DAC with full scale of 1V and maximum input signal frequency of 6 KHZ. Capture voltage waveforms at the significant circuit nodes to show operation of the circuit.

**Experiment 3 (Extra Credit):** Construct a voice recorder and player that will accepts voice signal from a microphone. Signal from the microphone would be converted to digital data by your 3-bit ADC designed in experiment #1. Then, the digitized signal would be converted back to analog form using DAC designed in experiment #2 and drive an audio speaker. Note that you need to amplify the signal from the microphone to match input range of the ADC and filter the DAC output to remove high frequency noise. Demonstrate operation to TA and capture voltage waveforms at the significant circuit nodes to show operation of the circuit.

**Post-Lab Deliverables:**
1) Submit your completed analysis of all experiments, measured data and the lesson learned from performing this lab.